

PRINT WINDOW CLOSE WINDOW

Search Result 31 of 34

◀ back next ▶

PAJ 00-66-76 04172537 JP **FAILURE ANALYSIS METHOD FOR INFORMATION PROCESSOR**

INVENTOR(S)- YOICHI, TSUFUKU; HIROHISA, NISHINE; HIROSHI, SHIGA; MAMORU, KANEKO

PATENT APPLICATION NUMBER- 02299716

DATE FILED- 1990-11-07

PUBLICATION NUMBER- 04172537 JP

DOCUMENT TYPE- A

PUBLICATION DATE- 1992-06-19

INTERNATIONAL PATENT CLASS- G06F01122

APPLICANT(S)- HITACHI LTD; HITACHI ELECTRON SERVICE CO LTD

PUBLICATION COUNTRY- Japan NDN- 190-0100-1972-9

11046 U.S. PTO
10/056495
01/28/02

PURPOSE: To enhance indicated resolution and precision of a defective part when the defect occurs by referring to a failure dictionary for parts including components of the processor, and by indicating a processor component part group included in a limited cover area as defective parts. **CONSTITUTION:** A failure dictionary 20 is prepared on the basis of a result of extracting in advance a cover area for total failure detecting circuit, and consists of a failure detecting circuit, processor components, and correspondence information for selector signals, cover for failure defecting circuit, information of connecting between logical elements included in the area, and so on. Failure analysis section 100 recognizes a leading light failure detecting circuit (FD) from a detected state of failure information 10, obtains bus selecting information from information 10 and the corresponding information of selector signals stored in dictionary 20, analyses the bus selecting information, and specifies a data transfer bus in the case of the occurrence of a failure. Failure analysis section 200 extracts a cover area from the content of the register of information 10 and inter-register connecting information. Failure analysis section 300 extracts a cover area for the case where a plurality of FDs exist. With this, a cover area is limited, thereby enhancing the indicated resolution and its accuracy. **COPYRIGHT:** (C)1992,JPO&Japio

NO-DESCRIPTORS

◀ back next ▶